REMARKS

Reconsideration and allowance of this application are respectfully requested in light of the above amendments and the following remarks.

Applicant acknowledges with appreciation the indication in the Office Action that claims 12-14 are allowable. Allowable claim 12 has been rewritten in independent form to include the subject matter of base claim 11. New claim 16 recites the subject matter of amended apparatus claim 12, but with respect to a method. Therefore, allowance of claims 12 and 16 and all claims dependent therefrom is warranted.

The Applicant wishes to thank the examiner for the courtesy extended to Applicant's representative during a telephone interview conducted on December 2, 2009. The participants were Examiner Rizk and David W. Ward, Reg. No. 45,198. During the interview, the examiner agreed that claims 12-14 and 16, as provided herein, would be allowed and that claims 11 and 15, as provided herein, distinguish over the applied reference of Xu et al. (US 7,210,089). The claims and prior art discussed are identified below. A summary of the substance of the issues discussed during the interview follows.

Claims 11 and 13-15 have been amended. Support for the amendments is provided in paragraph [0045] of the published specification. (It should be noted that references herein to the specification and drawings are for illustrative purposes only and are not intended to limit the scope of the invention to the referenced embodiments.)

Claims 11 and 15 were rejected, under 35 USC §102(e), as being anticipated by Xu. During the interview, these rejections were traversed as follows

Claim 11 now defines an input control apparatus that receives and performs dematching processing on a turbo encoded signal having bits of a systematic part and bits of parity parts. The input control apparatus discards systematic and parity bits of the received and dematched signal, prior to performing turbo decoding, such that the number of bits in each sequence of the parity parts is less than the number of bits in the systematic part. The claimed subject matter provides an advantage of reducing the number of bits required for performing a decoding calculation in a turbo decoder, so that the memory capacity required in this calculation is reduced and the circuit scale of the apparatus is reduced (see paragraphs [0014]-[0016] of the published specification).

The Office Action proposes that Xu discloses, in Fig. 3, components 35 and 37 that perform the operations described by Xu in column 7, lines 35-67, and that these operations are identical to the claimed operations mentioned above (see Office Action, sentence bridging pages 3 and 4).

However, Xu does not disclose that one or more components of the receiver illustrated in Fig. 3 perform the operations described in column 7, lines 35-67. Instead, Xu discloses that a rate matching unit 7 of the transmitter illustrated in Fig. 1 performs these operations (see Xu col. 7, lines 36-67).

Although Xu may disclose operations similar to those recited in claim 11, these operations are not performed after a rate dematching operation, as are the Applicant's claimed operations. Instead, Xu discloses that these operations constitute a rate matching operation (see Xu col. 7, lines 45-49).

Thus, Xu does not disclose the Applicant's claimed subject matter of discarding systematic and parity bits of a dematched signal, prior to performing turbo decoding, such that

the number of bits in each sequence of the parity parts is less than the number of bits in the systematic part.

Although Xu discloses a rate dematching unit 33 in Fig. 3 and components 35 and 37 that perform operations after the rate dematching, as proposed in the Office Action (see Office Action page 4, line 3), it should be noted that component 35 stores bits of multiple transmissions that it receives from rate dematching unit 33 and component 37 generates, from the accumulation of stored bits, a complete turbo encoded sequence comprising a systematic bit S and its accompanying parity bits P_1, P_2, P_3, and P_4, which are decoded by a turbo decoder 39 (see Xu col. 8, lines 47-55).

More specifically, Xu discloses communicating each of bits S, P_1, P_2, P_3, and P_4 in a separate transmission (see Xu col. 8, lines 3-23), and components 35 and 37 of the receiver illustrated in Fig. 3 regenerate the turbo encoded data sequence S, P_1, P_2, P_3, and P_4 from the multiple transmissions, for subsequent turbo decoding. As a result, Xu's components 35 and 37 accumulate individual bits into a data sequence, after a dematching operation, whereas the Applicant's claimed subject matter discards systematic and parity bits such that the number of bits in each sequence of the parity parts is less than the number of bits in the systematic part, after a dematching operation. For this reason, Xu does not identically disclose the instant claimed subject matter.

Accordingly, the Applicant submits that Xu does not anticipate the subject matter now defined by claim 11. Independent claim 15 now similarly recites the above-mentioned subject matter distinguishing apparatus claim 11 from Xu's disclosure, but with respect to a method. Therefore, allowance of claims 11 and 15 is deemed to be warranted.

In view of the above, it is submitted that this application is in condition for allowance, and a notice to that effect is respectfully solicited.

If any issues remain which may best be resolved through a telephone communication, the Examiner is requested to telephone the undersigned at the local Washington, D.C. telephone number listed below.

Respectfully submitted,

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